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**In the Claims**

Please cancel claims 3-7, 27, and 28. The claims are as follows:

1-7. (CANCELLED)

8. (Previously Presented) A method of testing a semiconductor chip having a plurality of common I/Os associated therewith, the method comprising the steps of:

connectivity testing a chip-to-package connection of at least one common I/O of the plurality of common I/Os, wherein said connectivity testing comprises generating a transition signal from a driver of the common I/O, and wherein the driver is configured as a weak driver that is sensitive to capacitive loading;

determining whether the chip-to-package connection is faulty from a result of the connectivity testing; and

placing an additional impedance into connection with the driver prior to generating the transition signal.

9. (Original) The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a resistor into series connection with the driver.

10. (Previously presented) The method of claim 8 further comprising electrically shorting the additional impedance from connection with the driver after generating the transition signal.

11. (Original) The method of claim 10, wherein electrically shorting the additional impedance includes completing a circuit around the additional impedance to bypass the additional impedance.

12-19. (Cancelled)

20. (Previously presented) The method of claim 9, wherein the resistor has an electrical resistance of at least 1 k $\Omega$ .

21. (Previously presented) The method of claim 9, wherein the resistor has an electrical resistance of at least 10 k $\Omega$ .

22. (Previously presented) The method of claim 9, wherein the resistor has an electrical resistance of at least 35 k $\Omega$ .

23. (Previously presented) The method of claim 9 wherein the resistor is electrically interposed between the driver and the common I/O.

24. (Previously presented) The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a field effect transistor(FET) into series connection with the driver.

25. (Previously presented) The method of claim 24, wherein the FET is electrically interposed between the driver and the common I/O.

26. (Previously presented) The method of claim 9, wherein the additional impedance is electrically interposed between the driver and the common I/O.

27. Cancelled

28. Cancelled